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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,925	01/09/2002	Thomas B. Berg	BEA920000022US1	3051

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IBM CORPORATION
IP LAW DEPT, ED02-905
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EXAMINER	
BULLOCK JR, LEWIS ALEXANDER	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,925	BERG ET AL.	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5/6/02.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: Page 1 and 2 details unreferenced serial numbers.

Appropriate correction is required.

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because it exceeds 150 words.

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by FRISCH (U.S. Patent 5,598,568).

As to claim 1, FRISCH teaches a method for handling resources of a multiprocessor system, comprising the steps of: a requestor group of one or more processors (requesting processor node / master node) of the system allocating a resource of a target group of one or more processors of the system (particular node / slave node) (col. 3, lines 56-67), the target being interconnected to the requestor (via the crossbar network), the resource being associated with a request of the requestor (via the transaction using the resource for execution) (col. 3, line 56 – col. 4, line 2); the requestor (master node) sending a result of the request to the target (slave node) (via the master communicating with the slave by using the address path of the memory location of the slave) (col. 4, line 25 – col. 5, line 2); and the target directly receiving the result by using the resource without intermediate handling of the resource by the target (via the master communicating with the slave by using the address path of the memory location of the slave) (col. 4, line 25 – col. 5, line 2; col. 5, lines 3-17).

As to claim 9, FRISCH teaches a computing system, comprising: a requestor group of one or more processors (requesting processor node / master node); a resource allocator (logic circuitry embedded in an application specific integrated circuit) responsive to requests of the requestor (col. 4, lines 3-18); and a target group of one or more processors (particular node / slave node) (col. 3, lines 56-67), the target being interconnected to the requestor (via the crossbar network) and responsive to a resource

provided by the resource allocator (allocated slave memory) and to a result of the request from the requestor (col. 4, lines 1-38); wherein the target directly receives the result responsive to the resource without intermediate handling of the resource by the target (via the master communicating with the slave by using the address path of the memory location of the slave) (col. 4, line 25 – col. 5, line 2; col. 5, lines 3-17).

As to claim 20, FRISCH teaches in a multiprocessor computer system comprising a plurality of processing nodes (master / slave nodes); a shared, distributed system memory (col. 3, lines 21-27); and a central hardware device (logic circuitry embedded in an application specific integrated circuit) comprising a communication pathway connecting the processing nodes (col. 4, lines 3-38); wherein each one of the processing nodes includes at least one processor (processor) (col. 3, lines 4-10); and a portion of the shared memory coupled to the processor and the communication pathway (local memory); the communication pathway (network) comprised of communications ports each dedicated to communicating with one of the processing nodes wherein the communications pathway is further comprised of a tag and address crossbar (crossbar network is made up of a plurality of communications ports for communicating over a plurality of paths) (col. 2, lines 57-67) to communicate tag and address information (path information), and a data crossbar means (a number of interconnected crossbars) to communicate data within the system (col. 2, lines 59-63); a method for handling tagging and addressing (path routing) within the system comprising the steps of: a first node (master node) communicating to the tag and address crossbar (crossbar) a request for

a transaction in the system(col. 3, lines 50-61); allocating a transaction identifier (via setting the crossbar interface registers) in the tag and address crossbar for use by the identified transaction (col. 4, line 3-55); attaching the transaction identifier (memory address / path) to the transaction (transaction); communicating the transaction from the first node (master node) to the node (slave node) which receives the transaction directly through the data crossing means (via an internal path or the path received) (col. 773, lines 1-65; col. 4, lines 56 – col. 5, line 2; col. 5, line 11-47; col. 1, line 60 – col. 2, line 13). It is inherent within the teachings of FRISCH that the master node has the transaction identifier in order to send the transaction over the path discovered in the routing registers.

As to claim 22, refer to claim 20 for rejection. However, claim 22 further details a central hardware device allocating resources of the target nodes for transactions and that the target node receives the results without intermediate buffering at the target node. FRISCH teaches a central hardware device (logic circuitry embedded in an application specific integrated circuit) allocating resources (allocating slave memory) of the target nodes for transactions (col. 4, lines 3-18) and that the target node receives the results without intermediate buffering at the target node (via the memory access instructions directly accessing a remote nodes memory) (col. 773, lines 49-54; col. 4, line 25 – col. 5, line 2; col. 5, lines 3-17).

As to claim 2, FRISCH teaches the requestor (master node) and the target (slave node) are interconnected by a central hardware device (logic circuitry embedded in an application specific integrated circuit); and the requestor sending a request to the central hardware device; and the central hardware device allocating the resource at the target group (col. 3, line 56 – col. 4, line 18).

As to claim 3, FRISCH teaches the central hardware device assigning an identifier to the request (via setting the register values) (col. 4, lines 3-55).

As to claim 4, FRISCH teaches the target deallocating the resource (via relinquish control of the resource to the master) (col. 3, line 50 – col. 4, line 2).

As to claim 5, FRISCH teaches the resource controls access to a portion of a shared system memory of the target (via the resource is a memory map system by which one node can access directly the memory of another through the crossbars) (col. 1, line 60 – col. 2, line 13; col. 3, line 62 – col. 4, line 2; col. 4, lines 56-67).

As to claims 6 and 7, FRISCH teaches the request is associated with a transaction between the requestor and the target (col. 3, line 56 – col. 4, line 2).

As to claim 8, FRISCH teaches the target comprising a first group and a second group of processors being interconnected (via the computer nodes having a plurality of processors) (col. 2, line 57 – col. 3, line 10).

As to claim 10, refer to claim 2 for rejection.

As to claim 11, FRISCH teaches one or more pipelines for handling requests (via one or more paths from one node to another) (col. 4, line 3 – col. 4, line 2; col. 773, lines 1-65).

As to claim 12, FRISCH teaches the central hardware device comprises a crossbar interconnecting the requestor and the target (col. 1, lines 60 - col. 2, line 13).

As to claim 13 and 14, FRISCH teaches the central hardware device comprises a plurality of crossbars for data interconnection and control interconnection (col. 1, line 60 – col. 2, line 13; col. 2, lines 57-67).

As to claim 15, FRISCH teaches the requestor and target are interconnected directly to each other (via the master node is able to directly access the slave node) (col. 1, line 60 – col. 2, line 13).

As to claims 16 and 17, FRISCH teaches the resource controls allocation of a portion of shared system memory of the target (via the resource is a memory map system by which one node can access directly the memory of another through the crossbars) (col. 1, line 60 – col. 2, line 13; col. 3, line 62 – col. 4, line 2; col. 4, lines 56-67).

As to claim 18 and 19, FRISCH teaches the target comprising a first group and a second group of processors being interconnected with the requestor (via the computer nodes having a plurality of processors and the master communicates with the slave) (col. 2, line 57 – col. 3, line 10; col. 3, lines 56-67).

As to claim 21, It is inherent within the teachings of FRISCH that the master node has the transaction identifier in order to send the transaction over the path discovered in the routing registers.

As to claim 23, FRISCH teaches the target node is comprised of more than one additional node (via the path refers to a list of crossbar ports) (col. 5, lines 18-40).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER

June 13, 2005